In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, lines 2 to 4 as follows:

B2 The technical field of this invention ~~provides~~ is a method of manipulating and processing display element data for scanned printer image buffers.

Rewrite the paragraph at page 1, line 7 to page 2, line 9as follows:

Printer page description languages (PDL), such as Postscript (a trademark of Adobe Systems Incorporated), use opaque image build up techniques to create the print page image. As new subimages are added to the image, the new subimage is written over the previous image within the boundary of the new subimage. These subimages are two dimensional regions which are mapped into memory space and B3 stored until the image creation is complete. This requires an image memory which is either addressable on display element boundaries or a memory which can be read, modified, and rewritten. The former requires image processors with narrow data bus widths which are not conducive to high speed data transfers. The ~~later~~ latter allows for high speed transfers but requires transfer of data which may not need to be modified.

Rewrite the paragraph at page 2, lines 17 to 28 as follows:

This invention is directed to a technique of image data processing. Image data is stored in a memory having data words of a predetermined data width. Each data word includes ~~a~~ plural B4 adjacently disposed image pixels of a single scan line. A set of consecutive data words corresponds to a two dimensional tile of the image whereby adjacent data words store image pixels of adjacent scan lines. The image data is transferred to a cache in these

tiles. Following image processing on a tile of image data stored in the cache, the tile of image data is transferred back to the memory. The technique repeats for each tile of image data. Separate tiles of image data may be operated on by different data processors simultaneously.

B4

Rewrite the paragraph at page 3, lines 4 to 5 as follows:

--Figure 1 illustrates ~~the~~ image data organization in the memory of this invention;--

B5

Rewrite the paragraph at page 3, lines 8 to 9 as follows:

--Figure 3 shows a block diagram of the TMS320C82 DSP (digital signal processor) in an image data processing system according to this invention.--

B6

Rewrite the paragraph at page 3, lines 12 to 21 as follows:

--The problem addressed by this invention is how to organize ~~the~~ an image memory for fast and efficient transfer of image data from ~~the~~ a processor to the image ~~storage~~ memory for read, modify, write applications. ~~This~~ In this invention, ~~uses~~ a processor with a wide data bus ~~which~~ can cache several words of data and organize the image memory in square tiles of display elements. This processor can cache small tiles of image memory, perform the intensive bit manipulations necessary and store the tile of display elements back to the image memory.--

B7

Rewrite the paragraph at page 3, line 28 to page 4, line 17 as follows:

--Figure 1 illustrates ~~the~~ image data organization in the memory 100 of this invention. For efficiency of memory space, display element data is packed into memory 100 as 16 pixels per long word of 64 data bits. The memory 100 is organized with 16 long words

B8

per tile starting on ~~a~~ modulo 128 address boundaries in the image display memory. The 64 bits in the first long word 101 in Tile 0 represent 16 adjacent pixels. The following long word 102 represents 16 pixels in the next ~~cross process~~ line of pixels directly below the pixels in the first long word. This sequence continues until 16 long words of pixel data has been defined ending with the 16 pixels of the sixteenth long word 116. The seventeenth long word 117, the first long word of the next tile, Tile 1, represents the 16 pixels adjacent in the ~~cross process direction~~ same line from the first long word in the ~~last~~ tile, Tile 0. This sequence continues until the far side of the image is included, then the sequence of tiles restarts 16 rows below the previous sequence of tiles. Note in Figure 1, the numbers within the boxes are the offset byte addresses from the beginning of the image in ~~Hexideeimal~~ Hexadecimal.--

Rewrite the paragraph at page 5, lines 8 to 19 as follows:

--Figure 2 illustrates in block diagram form an image data processor 200 implementing this invention. ~~This invention~~ Image data processor 200 includes image memory 201 storing the image to be processed. This image memory 201 has a pixel organization such as illustrated in Figure 1. Image data processor system 200 also includes one or more image processors 211 and 221. Each image processor 211 and 221 has a corresponding tile cache 213 and 223. The respective tile caches 213 and 223 are also connected to image processor system bus 205. Image processor system bus 205 is also connected to image memory 201 and may be connected to other image processor and tile cache combinations.--

Rewrite the paragraph at page 5, line 25 to page 6, line 10 as follows:

--For the sake of comparison, assume that a typical page of text is approximately 10% dense, that is, 1 in 10 display elements are part of the text strokes used to make the image. Using the prior art memory organization, access to display elements in one direction of the two dimensional array can be accomplished within a DRAM row, page mode access. However, display element access in the other direction must be random for images of any substantial size. Accesses within a DRAM (dynamic random access memory) row may be accomplished using page mode techniques which result in access times on the order of 50 nanoseconds per access, whereas non-page mode accesses, page miss accesses, require access times on the order of 150 nanoseconds. According to this prior art memory organization, randomly accessing 10% of 256 display elements at a time would require about 25.6 accesses or 3840 nanoseconds for write only operations.--

B10

Rewrite the paragraph at page 6, line 28 to page 7, line 10 as follows:

--The multiprocessor DSP is a single integrated circuit 180. Integrated circuit 180 is a fully programmable parallel processing platform that integrates two advanced DSP cores DSP 181 and DSP 182, a reduced instruction set computer (RISC) master processor (MP) 183, multiple static random access memory (SRAM) blocks 185, 186 and 187, a crossbar switch 184 that interconnects all the internal processors and memories, and a transfer controller (TC) 188 that controls external communications. Transfer controller 188 is coupled to image memory 190 via bus 195. Note that transfer controller 188 controls all data transfer between integrated circuit 180 and image memory 190. Image data is stored in image memory 190 in tiles as illustrated in Figure 1.

B11

Rewrite the paragraph at page 7, lines 11 to 25 as follows:

--In operation, the individual DSPs 181 and 182 ~~operated~~ operate independently on separate tiles. Each DSP 181 and 182 signals transfer controller 188 to transfer a tile of data from image memory 190 to the corresponding SRAM (static random access memory) 185 and 186. The DSPs 181 and 182 perform a programmed image transformation function on the tile data ~~in place in~~ within the corresponding SRAMs 185 and 186. Access by DSPs 181 and 182 and master processor 183 to SRAMs 185, 186 and 187 is mediated by crossbar switch 184. When complete, the DSPs 181 and 182 signal transfer controller 188 to transfer data back to image memory 190 for storage in the memory location allocated to the corresponding tile. This ~~cache-like~~ technique greatly reduces the memory transfer requirements of image memory 190. Master processor 183 is preferably programmed for high level functions such as communication with other parts not shown.----

B12